WE CLAIM:

Sub

1. A front-end processing system for a processor, comprising:

a UOP cache and an instruction cache, each having inputs coupled to a common addressing input, the UOP cache having an output for a hit/miss indicator,

an instruction processing system in communication with the instruction cache, having an enabling control input coupled to the hit/miss output of the UOP cache.

2. The front-end processing system of claim 1, wherein the instruction cache comprises a cache lookup unit and a cache fetch unit, the cache fetch unit having an enabling control input coupled to the hit/miss output of the UOP cache.

3. The front-end processing system of claim 1, wherein the instruction processing system comprises an instruction synchronizer and an instruction decoder coupled to each other.

4. The front-end processing system of claim 1, wherein the UOP cache comprises a cache lookup unit and a cache fetch unit, the cache lookup unit coupled to the hit/miss output.

5. The front-end processing system of claim 4, wherein the UOP cache further comprises a delay element provided between the cache lookup unit and the cache fetch unit.

6. The front-end processing system of claim 5, wherein the delay element is associated with a delay corresponding to a processing time of the instruction processing system.

7. A cache comprising:

a cache lookup unit,

a delay element coupled to the cache lookup unit, and

a data fetch unit coupled to the delay element.

8. The cache of claim 7, wherein the cache is populated by a plurality of cache entries and wherein the cache lookup unit comprises tag fields of the cache entries and a comparator coupled to the tag fields.

9. The cache of claim 8, wherein the cache is populated by a plurality of cache entries and wherein the cache lookup unit comprises tag fields of the cache entries and a comparator coupled to the tag fields.

10. A front-end processing system for a processor, comprising:

a UOP cache and an instruction cache, each having inputs coupled to a common addressing input, wherein the UOP cache includes an output for a hit/miss indicator,

wherein the instruction cache includes a cache lookup unit and a data fetch unit, the hit/miss indicator to selectively disable the data fetch unit.

11. The front-end system of claim 10, further comprising an instruction processing system in communication with the instruction cache, the hit/miss indicator to selectively disable the instruction processing system.

12. The front-end processing system of claim 11, wherein the instruction processing system comprises an instruction synchronizer and an instruction decoder coupled to each other.

13. The front-end processing system of claim 10, wherein the UOP cache comprises a cache lookup unit and a cache fetch unit, the cache lookup unit coupled to the hit/miss indicator.

14. The front-end processing system of claim 13, wherein the UOP cache further comprises a delay element provided between the cache lookup unit and the cache fetch unit, the delay element controlled by the hit/miss indicator.

15. The front-end processing system of claim 14, wherein the delay element is associated with a delay corresponding to a processing time of the instruction processing system.

16. A cache comprising a plurality of cache lines, each having fields to store tag data, offset data, a plurality of uops and byte length data, the offset data and the byte length data referring to source data in another cache.

17. The cache of claim 16, wherein the offset data represents an offset of a source instruction corresponding to a first UOP from the beginning of a cache line in which the source instruction is stored.

18. The cache of claim 16, wherein the byte length data represents a byte length of source instructions in the other cache to which the uops correspond.

Sub A1

19. The cache of claim 12, further comprising a field to store a next line pointer, indicating another way in the cache in which subsequent uops are likely to be found.

20. The cache of claim 12, wherein an offset field comprises a plurality of offset sub-fields, each sub-field corresponding to a UOP position in the cache line.

21. The cache of claim 20, further comprising a cache lookup unit, comprising a comparator, one coupled to each of the sub-fields and having an input for address data.

22. The cache of claim 21, wherein the cache line includes a single tag field coupled to each of the comparators.